CLAIMS

What is claimed is:

1. A controller chip comprising:

an engine for managing a memory and including an interface; and

a storage element coupled to the engine, the storage element being accessible by a central processing unit (CPU), wherein the engine receives commands from the CPU via the interface, manages the storage element and writes the commands into the memory.

2. The controller chip of claim 1 wherein the storage element comprises a first in first out (FIFO) buffer.

3. The controller chip of claim 2 in which the FIFO buffer comprises a circular FIFO buffer.

4. The controller chip of claim 2 in which the FIFO buffer comprises a double buffer.

5. The controller chip of claim 2 in which the FIFO buffer comprises a triple buffer.

6. The controller chip of claim 3 wherein the effective size of the FIFO buffer as

viewed by the CPU can be as large as the memory.

7. The controller chip of claim 2 which includes a checking mechanism for determining if the FIFO buffer needs to be emptied without utilizing the CPU.

8. The controller chip of claim 7 wherein the checking mechanism comprises:

means for calculating the time required to fill the FIFO buffer;

means for determining if the used memory of the FIFO buffer is below a predetermined amount based upon the time required to fill the FIFO buffer; and

means for preventing the FIFO buffer from filling if the used memory in the FIFO buffer is over the predetermined amount.

9. The controller chip of claim 1 wherein the controller chip comprises a graphics controller chip.

10. The controller chip of claim 9 wherein the engine comprises a graphics engine.

11. A system for providing a command stream in a computer system comprising:

a central processing unit (CPU);

a controller coupled to the CPU and including an interface;

a memory coupled to the controller, the memory being managed by the controller; and

a storage element coupled to the controller, the storage element being accessible by the CPU, wherein the controller receives commands from the CPU via the interface, manages the storage element and writes the commands into the memory.

12. The system of claim 11 wherein the storage element comprises a first in first out (FIFO) buffer.

13. The system of claim 12 in which the FIFO buffer comprises a circular FIFO buffer.

14. The system of claim 12 in which the FIFO buffer comprises a double buffer.

15. The system of claim 12 in which the FIFO buffer comprises a triple buffer.

16. The system of claim 12 in which the controller comprises a graphics controller.

17. The system of claim 12 wherein the effective size of the FIFO buffer can be as large as the memory.

18. The system of claim 12 which includes a checking mechanism for determining if the FIFO buffer needs to be emptied without utilizing the CPU.

19. The system of claim 18 wherein the checking mechanism comprises:

means for calculating the time required to fill the FIFO buffer;

means for determining if the FIFO buffer is below a predetermined amount based upon the time required to fill the buffer; and

means for preventing the FIFO buffer from filling if the FIFO buffer is above the predetermined amount.

20. A method for providing a command stream in a computer system, the computer system including a central processing unit (CPU), a controller coupled to the CPU, a memory coupled to the controller, the memory being managed by the controller; the method comprising the steps of:

(a) providing a storage element within the controller; and

(b) allowing the storage element to be accessible by the CPU via an interface in the graphics controller.

21. The method of claim 20 wherein the storage element comprises a FIFO buffer.

22. The method of claim 21 in which the FIFO buffer comprises a circular FIFO buffer.

23. The method of claim 21 in which the FIFO buffer comprises a double buffer.

24. The method of claim 21 in which the FIFO buffer comprises a triple buffer.

25. The method of claim 21 in which the memory comprises a graphics memory.

26. The method of claim 21 wherein the effective size of the FIFO buffer as viewed by the CPU can be as large as the memory.

27. The method of claim 21 which includes the step of (c) determining if the FIFO buffer needs to be emptied without utilizing the CPU.

28. The method of claim 27 wherein the determining step (c) further comprises:

(c1) calculating the time required to fill the FIFO buffer;

(c2) determining if the FIFO buffer is below a predetermined amount based upon the time required to fill the buffer; and

(c3) preventing the FIFO buffer from filling if the FIFO buffer is above the predetermined amount.